INTEGRATED CIRCUITS

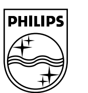
DATA SHEET

TEA6322T
Sound fader control circuit

Preliminary specification
File under Integrated Circuits, IC01

1995 Dec 19

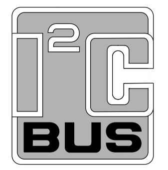
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FEATURES

- Source selector for three stereo and one differential stereo input for remote sources
- The differential stereo input works optional as a fourth stereo input and the common mode pin can be used as well as an additional mono input
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Output at volume I for external booster
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Logic output to read mute status
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset
- Power-down indication.



GENERAL DESCRIPTION

The sound fader control circuit TEA6322T is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		–86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		–15	–	+15	dB
G_{treble}	treble control		–12	–	+12	dB
$G_{step(treble)}$	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_O = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
CMRR	common mode rejection ratio differential stereo input		43	53	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6322T	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAM

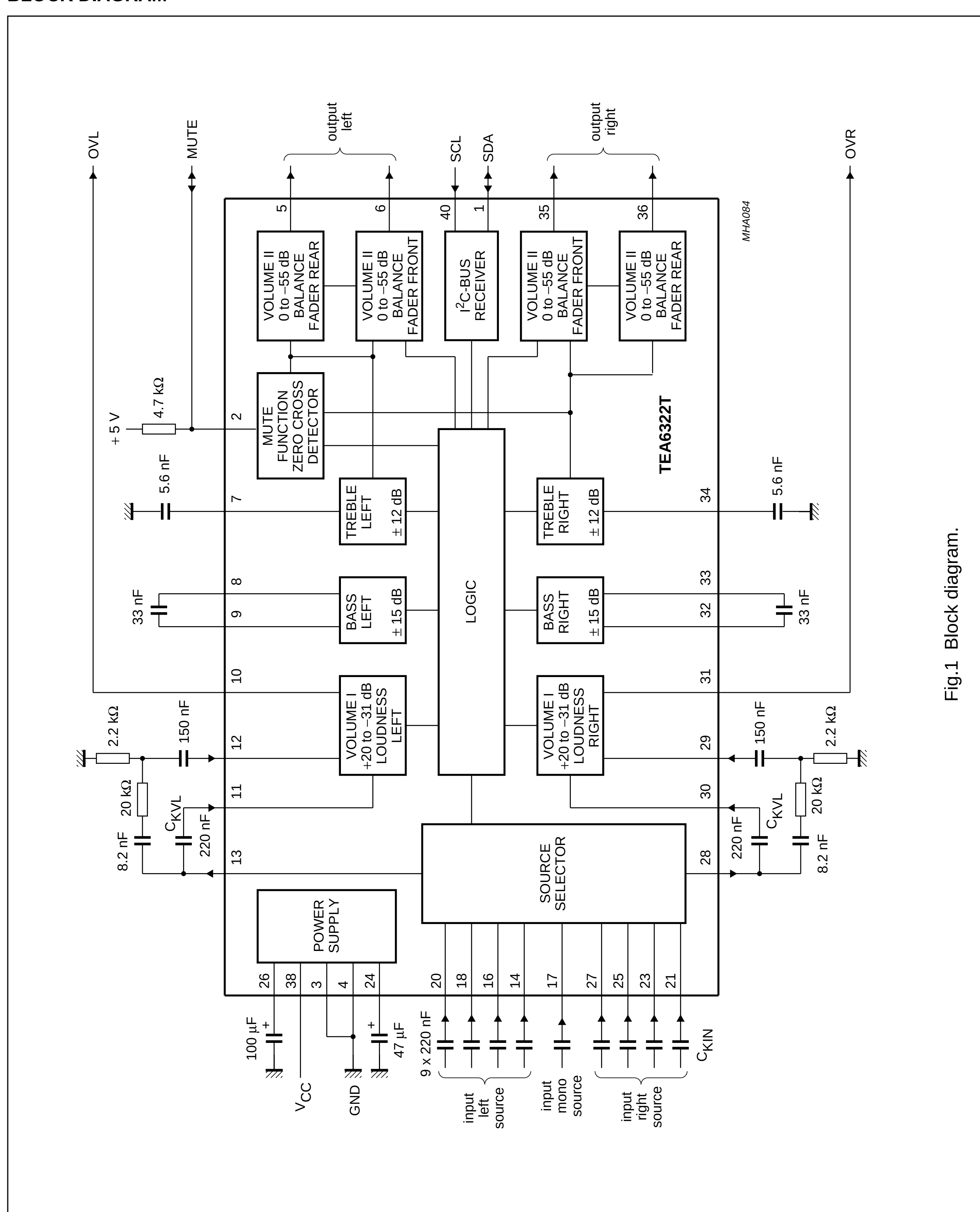


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
MUTE	2	mute control input and output
DGND	3	digital ground
AGND	4	analog ground
OUTLR	5	output left rear
OUTLF	6	output left front
TL	7	treble control capacitor left channel or input from external equalizer
B2L	8	bass control capacitor left channel or output to an external equalizer
B1L	9	bass control capacitor, left channel
OVL	10	output volume I, left channel
IVL	11	input volume I, left control part
ILL	12	input loudness, left control part
QSL	13	output source selector, left channel
IDL	14	input D left source
i.c.	15	COMM, common mode rejection adjust, centre position
ICL	16	input C left source
COM	17	common mode input / mono source input
IBL	18	input B left source
i.c.	19	COML, common mode rejection adjust, left position
IAL	20	input A differential source left
IAR	21	input A differential source right
i.c.	22	COMR, common mode rejection adjust, right position
IBR	23	input B right source
CAP	24	electronic filtering for supply
ICR	25	input C right source
V_{ref}	26	reference voltage (0.5 V_{CC})
IDR	27	input D right source
QSR	28	output source selector right channel
ILR	29	input loudness right channel
IVR	30	input volume I, right control part
OVR	31	output volume I, right channel
B1R	32	bass control capacitor right channel
B2R	33	bass control capacitor right channel or output to an external equalizer
TR	34	treble control capacitor right channel or input from an external equalizer
OUTRF	35	output right front
OUTRR	36	output right rear
n.c.	37	not connected
V_{CC}	38	supply voltage
n.c.	39	not connected
SCL	40	serial clock input

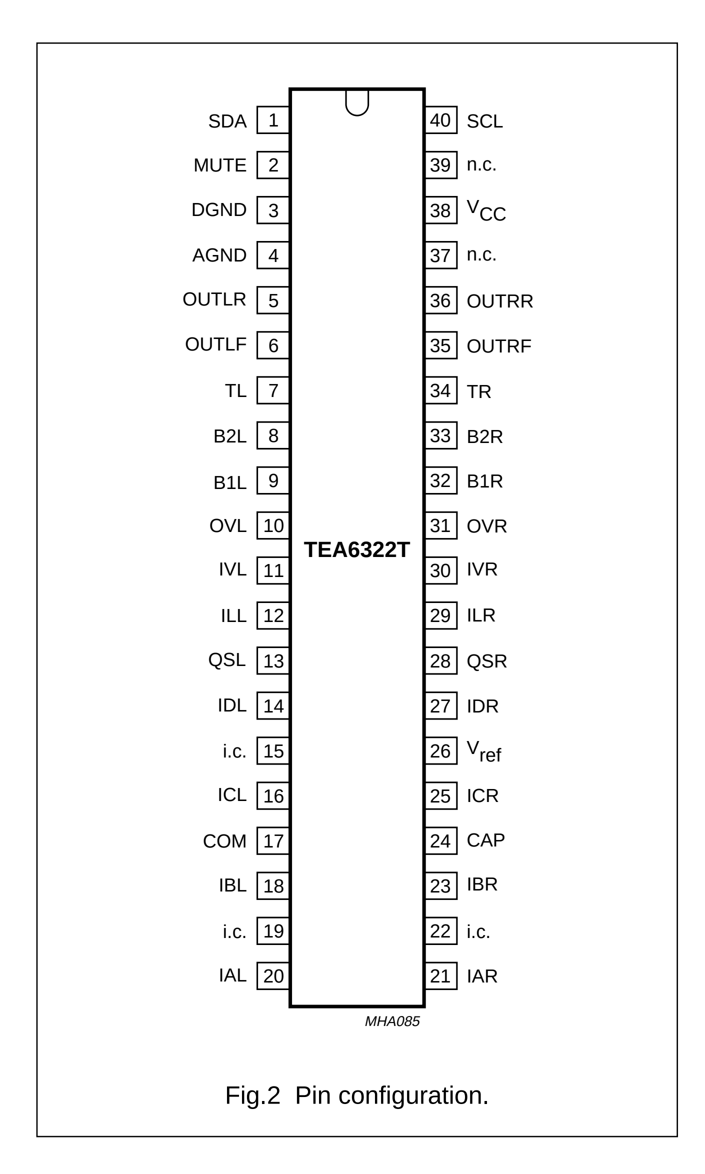


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The source selector allows either the source selection between the differential stereo input (IAL, IAR and COM) and three stereo inputs, or selection of four stereo inputs and the mono input (COM). The maximum input signal voltage is $V_{i(rms)}$ = 2 V. The outputs of the source selector and the inputs of the following volume control parts are available at pins 13 and 11 for the left channel and pins 28 and 30 for the right channel. This offers the possibility of interfacing a noise reduction system.

The volume control part is following the source selector. The signal phase from input volume control part to all outputs is 180°.

The volume control function is split into two sections: volume I control block and volume II control block.

The control range of volume I is between +20 dB and –31 dB in steps of 1 dB. The volume II control range is between 0 dB and –55 dB in steps of 1 dB. Although the theoretical possible control range is 106 dB (+20 to –86 dB), in practice a range of 86 dB (+20 to –66 dB) is recommended. The gain/attenuation setting of the volume I control block is common for both channels.

The volume I control block operates in combination with the loudness control. The filter is linear when the maximum gain for the volume I control (+20 dB) is selected. The filter characteristic increases automatically over a range of 32 dB down to a setting of –12 dB. That means the maximum filter characteristic is obtained at –12 dB setting of volume I. Further reduction of the volume does not further influence the filter characteristic (see Fig.5). The maximum selected filter characteristic is determined by external components. The proposed application gives a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via I^2C-bus control (see Table 7).

The volume I control block has an output pin and is followed by the bass control block. A single external capacitor of 33 nF for each channel in combination with internal resistors, provides the frequency response of the bass control (see Fig.3). The adjustable range is between –15 and +15 dB at 40 Hz.

Both loudness and bass control result in a maximum bass boost of 32 dB for low volume settings.

The treble control block offers a control range between –12 and +12 dB in steps of 1.5 dB at 15 kHz. The filter characteristic is determined by a single capacitor of 5.6 nF for each channel in combination with internal resistors (see Fig.4).

The basic step width of bass and treble control is 3 dB. The intermediate steps are obtained by switching 1.5 dB boost and 1.5 dB attenuation steps.

The bass and treble control functions can be switched off via I^2C-bus. In this event the internal signal flow is disconnected. The connections B2L and B2R are outputs and TL and TR are inputs for inserting an external equalizer.

The last section of the circuit is the volume II block. The balance and fader functions are performed using the same control blocks. This is realized by 4 independently controllable attenuators, one for each output. The control range of these attenuators is 55 dB in steps of 1 dB with an additional mute step.

The circuit provides 3 mute modes:

1. Zero crossing mode mute via I^2C-bus using 2 independent zero crossing detectors (ZCM, see Tables 2 and 9).
2. Fast mute via MUTE pin.
3. Fast mute via I^2C-bus either by general mute (GMU, see Tables 2 and 9) or volume II block setting (see Table 4).

The mute function is performed immediately if ZCM is cleared (ZCM = 0). If the bit is set (ZCM = 1) the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. As the two audio channels (left and right) are independent, two comparators are built-in to control independent mute switches.

To avoid a large delay of mute switching when very low frequencies are processed or the output signal amplitude is lower than the DC offset voltage a second I^2C-bus transmission is needed. Both transmissions have the same data and the second transmission a delay time of e.g. 100 ms. The first transmission starts the zero cross circuit, but second transmission moves the mute switch immediately if the circuit has no zero cross detected.

The mute function can also be controlled externally. If the mute pin is switched to ground all outputs are muted immediately (except the outputs volume left and right (OVL and OVR) and hardware mute). This mute request overwrites all mute controls via the I^2C-bus for the time the pin is held LOW. The hardware mute position is not stored in the TEA6322T.

The MUTE pin can also be used as output. The mute pin voltage is LOW when all outputs are in mute position.

For the turn on/off behaviour the following explanation is generally valid. To avoid AF output caused by the input signal coming from preceding stages, which produces output during drop of V_{CC}, the mute has to be set, before the V_{CC} will drop. This can be achieved by I^2C-bus control or by grounding the MUTE pin.

For use where is no mute in the application before turn off, a supply voltage drop of more than $1 \times V_{BE}$ will result in a mute during the voltage drop.

The power supply should include a V_{CC} buffer capacitor, which provides a discharging time constant. If the input signal does not disappear after turn off the input will become audible after certain time. A 4.7 kΩ resistor discharges the V_{CC} buffer capacitor, because the internal current of the IC does not discharge it completely.

The hardware mute function is favourable for use in Radio Data System (RDS) applications. The zero crossing mute avoids modulation plops. This feature is an advantage for mute during changing presets and/or sources (e.g. traffic announcement during cassette playback).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
V_n	voltage at pins 1, 2 and 5 to 40 to pins 3 and 4		0	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling	note 1			

Note

1. Human body model: C = 100 pF; R = 1.5 kΩ; V ≥ 2 kV. Charge device model: C = 200 pF; R = 0 Ω; V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 8.5 V; R_S = 600 Ω; R_L = 10 kΩ; C_L = 2.5 nF; AC coupled; f = 1 kHz; T_{amb} = 25 °C; gain control G_v = 0 dB; bass linear; treble linear; fader off; balance in mid position; loudness off; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current		–	26	33	mA
V_{DC}	internal DC voltage at inputs and outputs		3.83	4.25	4.68	V
V_{ref}	internal reference voltage at pin 26		–	4.25	–	V
$G_{v(max)}$	maximum voltage gain	R_S = 0 Ω; R_L = ∞	19	20	21	dB
$V_{o(rms)}$	output voltage level for					
	P_{max} at the power output stage	THD ≤ 0.5%; see Fig.10	–	2000	–	mV
	start of clipping	THD = 1%; G_v = 3 dB	2300	–	–	mV
		R_L = 2 kΩ; C_L = 10 nF; THD = 1%	2000	–	–	mV
$V_{i(rms)}$	input sensitivity	V_o = 2000 mV; G_v = 20 dB	–	200	–	mV
f_{ro}	roll-off frequency	C_{KIN} = 220 nF; C_{KVL} = 220 nF; Z_i = $Z_{i(min)}$				
		low frequency (–1 dB)	60	–	–	Hz
		low frequency (–3 dB)	30	–	–	Hz
		high frequency (–1 dB)	20000	–	–	Hz
		C_{KIN} = 470 nF; C_{KVL} = 100 nF; Z_i = $Z_{i(typ)}$ low frequency (–3 dB)	17	–	–	Hz
α_{cs}	channel separation	V_i = 2 V; frequency range 250 Hz to 10 kHz	74	80	–	dB
THD	total harmonic distortion	frequency range 20 Hz to 12.5 kHz				
		V_i = 100 mV; G_v = 20 dB	–	0.1	–	%
		V_i = 1 V; G_v = 0 dB	–	0.05	0.1	%
		V_i = 2 V; G_v = 0 dB	–	0.1	–	%
		V_i = 2 V; G_v = –10 dB	–	0.1	–	%
RR	ripple rejection	$V_{r(rms)}$ < 200 mV				
		f = 100 Hz	70	76	–	dB
		f = 40 Hz to 12.5 kHz	–	66	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(S+N)/N	signal-plus-noise to noise ratio	unweighted; 20 Hz to 20 kHz (RMS); V_o = 2.0 V; see Figs 6 and 7	–	105	–	dB
		CCIR468-2 weighted; quasi peak; V_o = 2.0 V				
		G_v = 0 dB	–	95	–	dB
		G_v = 12 dB	–	88	–	dB
		G_v = 20 dB	–	81	–	dB
		differential input				
		G_v = 0 dB	–	90	–	dB
		G_v = 20 dB	–	79	–	dB
CMRR	common mode rejection ratio differential stereo input		43	53	–	dB
$P_{no(rms)}$	noise output power (RMS value) only contribution of TEA6322T; power amplifier for 6 W	mute position; note 1	–	–	10	nW
α_{ct}	crosstalk $\left(20\ \log\frac{V_{bus(p-p)}}{V_{o(rms)}}\right)$ between bus inputs and signal outputs	note 2	–	110	–	dB
Source selector						
Z_i	input impedance		25	35	45	kΩ
α_S	input isolation of one selected source to any other input	f = 1 kHz	–	105	–	dB
		f = 12.5 kHz	–	95	–	dB
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%; V_{CC} = 8.5 V	–	2.15	–	V
		THD < 0.5%; V_{CC} = 7.5 V	–	1.8	–	V
V_{offset}	DC offset voltage at source selector output					
	by selection of any stereo inputs		–	–	10	mV
	by selection of differential input or mono input		–	–	20	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		10	–	–	kΩ
C_L	output load capacity		0	–	2500	pF
G_v	voltage gain, source selector		–	0	–	dB
Control part (source selector disconnected; source resistance 600 Ω)						
Z_i	input impedance volume input		100	150	200	kΩ
	input impedance loudness input		25	33	40	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		2	–	–	kΩ
C_L	output load capacity		0	–	10	nF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	–	2.15	–	V
V_{no}	noise output voltage	CCIR468-2 weighted; quasi peak				
		G_v = 20 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		G_v = –66 dB	–	13	22	μV
		mute position	–	10	–	μV
CR_{tot}	total continuous control range		–	106	–	dB
	recommended control range		–	86	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_v = +20 to –50 dB	–	–	2	dB
		G_v = –51 to –66 dB	–	–	3	dB
ΔG_t	gain tracking error	G_v = +20 to –50 dB	–	–	2	dB
$MUTE_{att}$	mute attenuation	see Fig.9	100	110	–	dB
V_{offset}	DC step offset between any adjoining step	G_v = 0 to –66 dB	–	0.2	10	mV
		G_v = 20 to 0 dB	–	2	15	mV
	DC step offset between any step to mute	G_v = 0 to –66 dB	–	–	10	mV
		G_v = 20 to 0 dB	–	–	40	mV
		G_v = 0 to –31 dB; loudness on	–	–	17	mV
Volume I control and loudness						
CR_{vol}	continuous volume control range		–	51	–	dB
G_v	voltage gain		–31	–	+20	dB
G_{step}	step resolution		–	1	–	dB
L_{Bmax}	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control						
G_{bass}	bass control, maximum boost	f = 40 Hz	14	15	16	dB
	maximum attenuation	f = 40 Hz	14	15	16	dB
G_{step}	step resolution (toggle switching)	f = 40 Hz	–	1.5	–	dB
	step error between any adjoining step	f = 40 Hz	–	–	0.5	dB
V_{offset}	DC step offset in any bass position		–	–	20	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Treble control						
G_{treble}	treble control, maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution (toggle switching)	f = 15 kHz	–	1.5	–	dB
	step error between any adjoining step	f = 15 kHz	–	–	0.5	dB
V_{offset}	DC step offset in any treble position		–	–	10	mV
Volume II, balance and fader control						
CR	continuous attenuation fader and volume control range		53.5	55	56.5	dB
G_{step}	step resolution		–	1	2	dB
	attenuation set error		–	–	1.5	dB
Mute function						
$V_{muteLOWI}$	input level for fast mute detection		–	–	1.0	V
	input level for no mute detection		2.2	–	–	V
$V_{muteLOWO}$	output level for mute	$I \leq 1$ mA; $C_L \leq 100$ pF	–	–	0.4	V
$V_{muteHIGH}$	pull-up voltage	open collector	–	–	V_{CC}	V
V_{CCdrop}	supply drop to V_{CAP} for mute active		–	–0.7	–	V
Power-on reset (when reset is active the GMU-bit (general mute) is set and the I²C-bus receiver is in reset position)						
V_{CC}	increasing supply voltage start of reset		–	–	2.5	V
	end of reset		5.2	6.5	7.2	V
	decreasing supply voltage start of reset		4.2	5.5	6.2	V
Digital part (I²C-bus pins); note 3						
V_{iH}	HIGH level input voltage		3	–	9.5	V
V_{iL}	LOW level input voltage		–0.3	–	+1.5	V
I_{iH}	HIGH level input current	V_{CC} = 0 to 9.5 V	–10	–	+10	μA
I_{iL}	LOW level input current		–10	–	+10	μA
V_{oL}	LOW level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier at 4 Ω with 20 dB gain and a fixed attenuator of 12 dB in front of it. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. The transmission contains: total initialization with MAD and subaddress for volume and 8 data words, see also definition of characteristics, clock frequency = 50 kHz, repetition burst rate = 400 Hz, maximum bus signal amplitude = 5 V (p-p).
3. The AC characteristics are in accordance with the I^2C-bus specification. This specification, "*The I²C-bus and how to use it*", can be ordered using the code 9398 393 40011.

I^2C-BUS PROTOCOL

I^2C-bus format

S(1)	SLAVE ADDRESS(2)	A(3)	SUBADDRESS(4)	A(3)	DATA(5)	A(3)	P(6)

Notes

1. S = START condition.
2. SLAVE ADDRESS (MAD) = 1000 0000.
3. A = acknowledge, generated by the slave.
4. SUBADDRESS (SAD), see Table 1.
5. DATA, see Table 1; if more than 1 byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.
6. P = STOP condition.

Table 1 Second byte after MAD

FUNCTION	BIT	MSB							LSB
		7	**6**	**5**	**4**	**3**	**2(1)**	**1(1)**	**0(1)**
Volume/loudness	V	0	0	0	0	0	0	0	0
Fader front right	FFR	0	0	0	0	0	0	0	1
Fader front left	FFL	0	0	0	0	0	0	1	0
Fader rear right	FRR	0	0	0	0	0	0	1	1
Fader rear left	FRL	0	0	0	0	0	1	0	0
Bass	BA	0	0	0	0	0	1	0	1
Treble	TR	0	0	0	0	0	1	1	0
Switch	S	0	0	0	0	0	1	1	1

Note

1. Significant subaddress.

Table 2 Definition of third byte after MAD and SAD

FUNCTION	BIT	MSB							LSB
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Volume/loudness	V	ZCM(1)	LOFF(2)	V5(3)	V4(3)	V3(3)	V2(3)	V1(3)	V0(3)
Fader front right	FFR	0	0	FFR5(5)	FFR4(5)	FFR3(5)	FFR2(5)	FFR1(5)	FFR0(5)
Fader front left	FFL	0	0	FFL5(6)	FFL4(6)	FFL3(6)	FFL2(6)	FFL1(6)	FFL0(6)
Fader rear right	FRR	0	0	FRR5(7)	FRR4(7)	FRR3(7)	FRR2(7)	FRR1(7)	FRR0(7)
Fader rear left	FRL	0	0	FRL5(8)	FRL4(8)	FRL3(8)	FRL2(8)	FRL1(8)	FRL0(8)
Bass	BA	0	0	0	BA4(9)	BA3(9)	BA2(9)	BA1(9)	BA0(9)
Treble	TR	0	0	0	TR4(10)	TR3(10)	TR2(10)	TR1(10)	TR0(10)
Switch	S	GMU(11)	0	0	0	0	SC2(12)	SC1(12)	SC0(12)

Notes

1. Zero crossing mode.
2. Switch loudness on/off.
3. Volume control.
4. Don’t care bits (logic 1 during testing).
5. Fader control front right.
6. Fader control front left.
7. Fader control rear right.
8. Fader control rear left.
9. Bass control.
10. Treble control.
11. Mute control for all outputs except OVL and OVR (general mute).
12. Source selector control.

Table 3 Volume I setting

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
Loudness on: the increment of the loudness characteristics is linear at every volume step in the range from +20 to –11 dB						
+20	1	1	1	1	1	1
+19	1	1	1	1	1	0
+18	1	1	1	1	0	1
+17	1	1	1	1	0	0
+16	1	1	1	0	1	1
+15	1	1	1	0	1	0
+14	1	1	1	0	0	1
+13	1	1	1	0	0	0
+12	1	1	0	1	1	1
+11	1	1	0	1	1	0
+10	1	1	0	1	0	1
+9	1	1	0	1	0	0
+8	1	1	0	0	1	1
+7	1	1	0	0	1	0
+6	1	1	0	0	0	1
+5	1	1	0	0	0	0
+4	1	0	1	1	1	1
+3	1	0	1	1	1	0
+2	1	0	1	1	0	1
+1	1	0	1	1	0	0
0	1	0	1	0	1	1
–1	1	0	1	0	1	0
–2	1	0	1	0	0	1
–3	1	0	1	0	0	0
–4	1	0	0	1	1	1
–5	1	0	0	1	1	0
–6	1	0	0	1	0	1
–7	1	0	0	1	0	0
–8	1	0	0	0	1	1
–9	1	0	0	0	1	0
–10	1	0	0	0	0	1
–11	1	0	0	0	0	0

G_v (dB)	DATA					
	V5	**V4**	**V3**	**V2**	**V1**	**V0**
Loudness characteristic is constant in a range from –11 dB to –31 dB						
–12	0	1	1	1	1	1
–13	0	1	1	1	1	0
–14	0	1	1	1	0	1
–15	0	1	1	1	0	0
–16	0	1	1	0	1	1
–17	0	1	1	0	1	0
–18	0	1	1	0	0	1
–19	0	1	1	0	0	0
–20	0	1	0	1	1	1
–21	0	1	0	1	1	0
–22	0	1	0	1	0	1
–23	0	1	0	1	0	0
–24	0	1	0	0	1	1
–25	0	1	0	0	1	0
–26	0	1	0	0	0	1
–27	0	1	0	0	0	0
–28	0	0	1	1	1	1
–29	0	0	1	1	1	0
–30	0	0	1	1	0	1
–31	0	0	1	1	0	0
Repetition of steps in a range from –28 dB to –31 dB						
–28	0	0	1	0	1	1
–29	0	0	1	0	1	0
–30	0	0	1	0	0	1
–31	0	0	1	0	0	0
–28	0	0	0	1	1	1
–29	0	0	0	1	1	0
–30	0	0	0	1	0	1
–31	0	0	0	1	0	0
–28	0	0	0	0	1	1
–29	0	0	0	0	1	0
–30	0	0	0	0	0	1
–31	0	0	0	0	0	0

Table 4 Volume II setting (fader and balance)

G_v (dB)	DATA					
	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
0	1	1	1	1	1	1
–1	1	1	1	1	1	0
–2	1	1	1	1	0	1
–3	1	1	1	1	0	0
–4	1	1	1	0	1	1
–5	1	1	1	0	1	0
–6	1	1	1	0	0	1
–7	1	1	1	0	0	0
–8	1	1	0	1	1	1
–9	1	1	0	1	1	0
–10	1	1	0	1	0	1
–11	1	1	0	1	0	0
–12	1	1	0	0	1	1
–13	1	1	0	0	1	0
–14	1	1	0	0	0	1
–15	1	1	0	0	0	0
–16	1	0	1	1	1	1
–17	1	0	1	1	1	0
–18	1	0	1	1	0	1
–19	1	0	1	1	0	0
–20	1	0	1	0	1	1
–21	1	0	1	0	1	0
–22	1	0	1	0	0	1
–23	1	0	1	0	0	0
–24	1	0	0	1	1	1
–25	1	0	0	1	1	0
–26	1	0	0	1	0	1
–27	1	0	0	1	0	0
–28	1	0	0	0	1	1
–29	1	0	0	0	1	0
–30	1	0	0	0	0	1
–31	1	0	0	0	0	0
–32	0	1	1	1	1	1
–33	0	1	1	1	1	0
–34	0	1	1	1	0	1

G_v (dB)	DATA					
	FRR5	**FRR4**	**FRR3**	**FRR2**	**FRR1**	**FRR0**
	FRL5	**FRL4**	**FRL3**	**FRL2**	**FRL1**	**FRL0**
	FFL5	**FFL4**	**FFL3**	**FFL2**	**FFL1**	**FFL0**
	FFR5	**FFR4**	**FFR3**	**FFR2**	**FFR1**	**FFR0**
–35	0	1	1	1	0	0
–36	0	1	1	0	1	1
–37	0	1	1	0	1	0
–38	0	1	1	0	0	1
–39	0	1	1	0	0	0
–40	0	1	0	1	1	1
–41	0	1	0	1	1	0
–42	0	1	0	1	0	1
–43	0	1	0	1	0	0
–44	0	1	0	0	1	1
–45	0	1	0	0	1	0
–46	0	1	0	0	0	1
–47	0	1	0	0	0	0
–48	0	0	1	1	1	1
–49	0	0	1	1	1	0
–50	0	0	1	1	0	1
–51	0	0	1	1	0	0
–52	0	0	1	0	1	1
–53	0	0	1	0	1	0
–54	0	0	1	0	0	1
–55	0	0	1	0	0	0
mute	0	0	0	1	1	1
mute	0	0	0	1	1	0
mute	0	0	0	1	0	1
mute	0	0	0	1	0	0
mute	0	0	0	0	1	1
mute	0	0	0	0	1	0
mute	0	0	0	0	0	1
mute	0	0	0	0	0	0

Table 5 Bass setting

G_{bass} (dB)	DATA				
	BA4	BA3	BA2	BA1	BA0
+15.0	1	1	1	1	1
+13.5	1	1	1	1	0
+15.0	1	1	1	0	1
+13.5	1	1	1	0	0
+15.0	1	1	0	1	1
+13.5	1	1	0	1	0
+12.0	1	1	0	0	1
+10.5	1	1	0	0	0
+9.0	1	0	1	1	1
+7.5	1	0	1	1	0
+6.0	1	0	1	0	1
+4.5	1	0	1	0	0
+3.0	1	0	0	1	1
+1.5	1	0	0	1	0
0(1)	1	0	0	0	1
0(2)	1	0	0	0	0
–1.5	0	1	1	1	1
–3.0	0	1	1	1	0
–4.5	0	1	1	0	1
–6.0	0	1	1	0	0
–7.5	0	1	0	1	1
–9.0	0	1	0	1	0
–10.5	0	1	0	0	1
–12.0	0	1	0	0	0
–13.5	0	0	1	1	1
–15.0	0	0	1	1	0
–13.5	0	0	1	0	1
–15.0	0	0	1	0	0
note 3	0	0	0	1	1
note 3	0	0	0	1	0
note 3	0	0	0	0	1
notes 3 and 4	0	0	0	0	0

Notes

1. Recommended data word for step 0 dB.
2. Result of 1.5 dB boost and 1.5 dB attenuation.
3. The last four bass control data words mute the bass response.
4. The last bass control and treble control data words (00000) enable the external equalizer connection.

Table 6 Treble setting

G_{treble} (dB)	DATA				
	TR4	**TR3**	**TR2**	**TR1**	**TR0**
+12.0	1	1	1	1	1
+10.5	1	1	1	1	0
+12.0	1	1	1	0	1
+10.5	1	1	1	0	0
+12.0	1	1	0	1	1
+10.5	1	1	0	1	0
+12.0	1	1	0	0	1
+10.5	1	1	0	0	0
+9.0	1	0	1	1	1
+7.5	1	0	1	1	0
+6.0	1	0	1	0	1
+4.5	1	0	1	0	0
+3.0	1	0	0	1	1
+1.5	1	0	0	1	0
0(1)	1	0	0	0	1
0(2)	1	0	0	0	0
–1.5	0	1	1	1	1
–3.0	0	1	1	1	0
–4.5	0	1	1	0	1
–6.0	0	1	1	0	0
–7.5	0	1	0	1	1
–9.0	0	1	0	1	0
–10.5	0	1	0	0	1
–12.0	0	1	0	0	0
note 3	0	0	1	1	1
note 3	0	0	1	1	0
note 3	0	0	1	0	1
note 3	0	0	1	0	0
note 3	0	0	0	1	1
note 3	0	0	0	1	0
note 3	0	0	0	0	1
notes 3 and 4	0	0	0	0	0

Notes

1. Recommended data word for step 0 dB.
2. Result of 1.5 dB boost and 1.5 dB attenuation.
3. The last eight treble control data words select treble output.
4. The last treble control and bass control data words (00000) enable the external equalizer connection.

Table 7 Loudness setting

CHARACTERISTIC	DATA LOFF
With loudness	0
Linear	1

Table 8 Selected input

FUNCTION	DATA		
	SC2	SC1	SC0
Stereo inputs IAL and IAR	1	1	1
Stereo inputs IBL and IBR	1	1	0
Stereo inputs ICL and ICR	1	0	1
Stereo inputs IDL and IDR	1	0	0
(Stereo inputs) IAL and IAR	0	1	1
Differential inputs IAL, IAR and COM	0	1	0
No input (input mute)	0	0	1
Mono input COM	0	0	0

Table 9 Mute mode

FUNCTION	DATA	
	GMU	ZCM
Direct mute off	0	0
Mute off delayed until the next zero crossing	0	1
Direct mute	1	0
Mute delayed until the next zero crossing	1	1

MED423

G_{bass} (dB)

18, 12, 6, 0, –6, –12, –18

10, 10^2, 10^3, f (Hz), 10^4

Fig.3 Bass control.

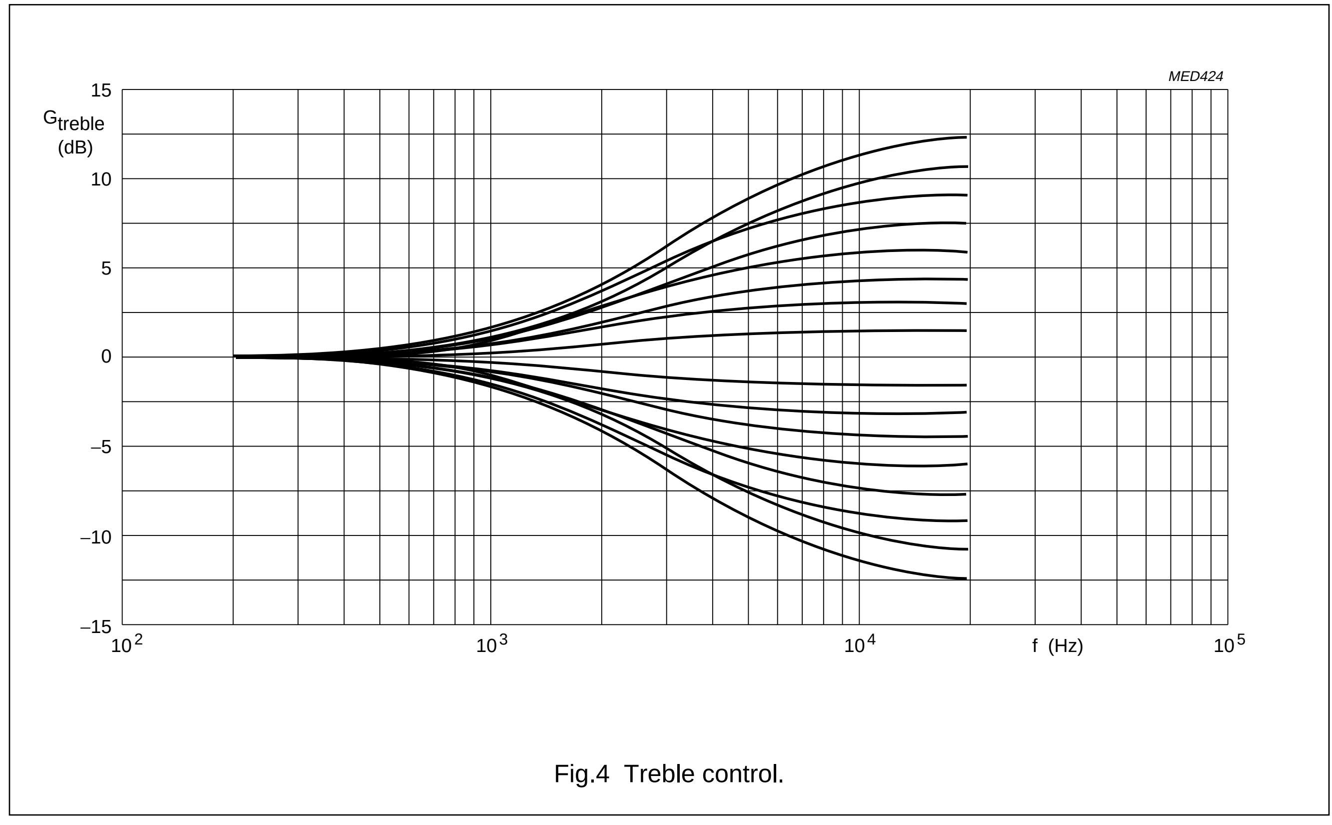


Fig.4 Treble control.

Fig.5 Volume control with loudness (including low roll-off frequency).

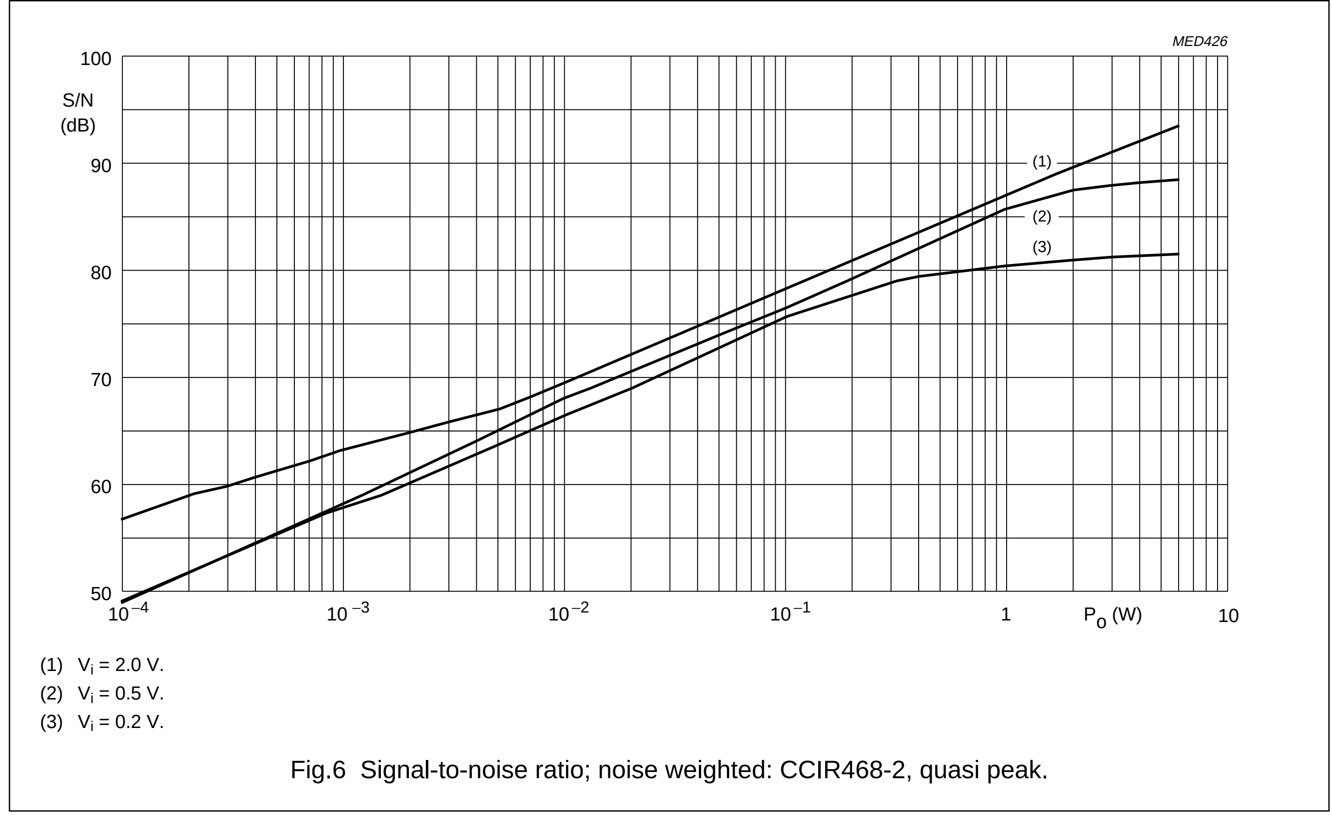
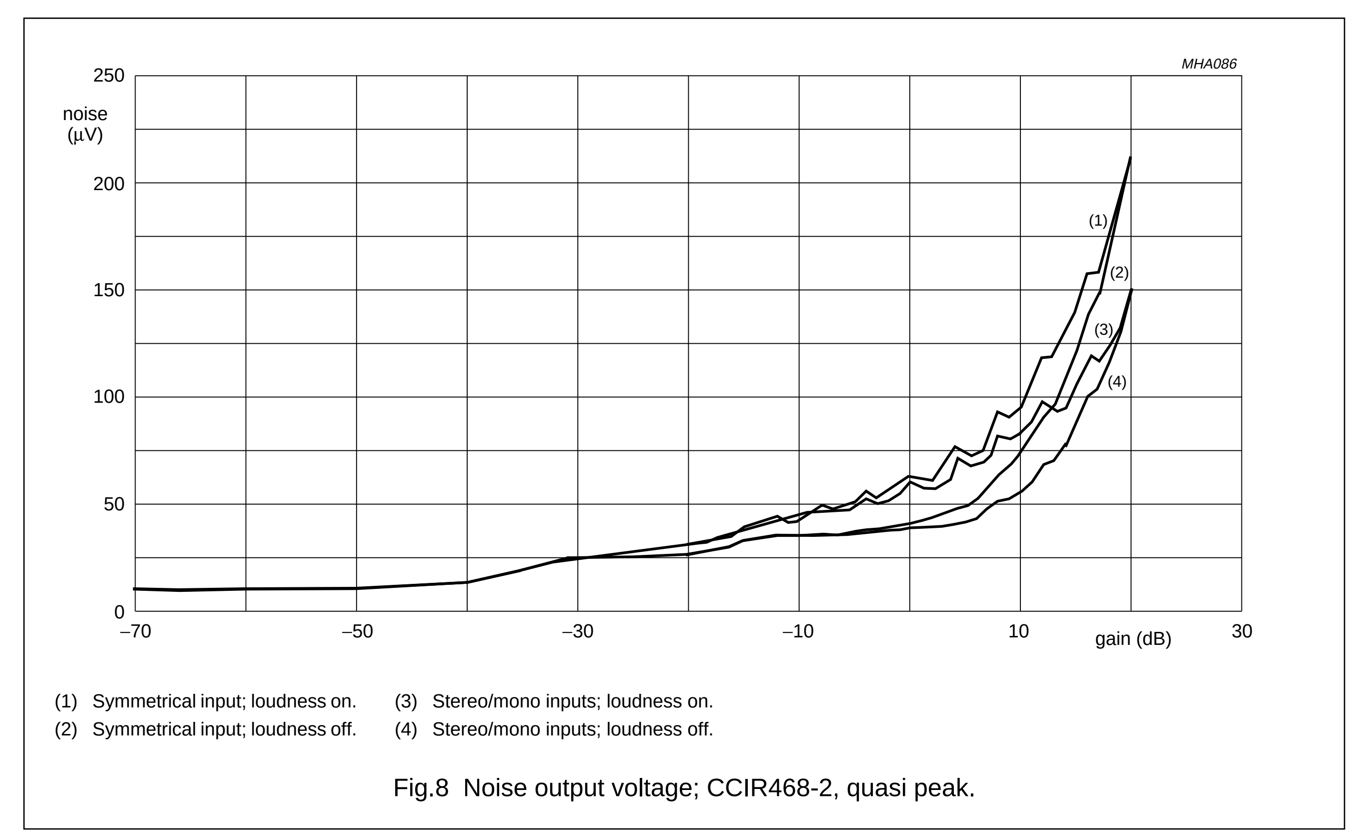


Fig.6 Signal-to-noise ratio; noise weighted: CCIR468-2, quasi peak.

(1) Unweighted RMS.
(2) CCIR-468-2 RMS.
(3) CCIR-468-2 quasi-peak.

Fig.7 Signal-to-noise ratio; V_i = 2 V; P_{max} = 6 W.



(1) Symmetrical input; loudness on.
(2) Symmetrical input; loudness off.
(3) Stereo/mono inputs; loudness on.
(4) Stereo/mono inputs; loudness off.

Fig.8 Noise output voltage; CCIR468-2, quasi peak.

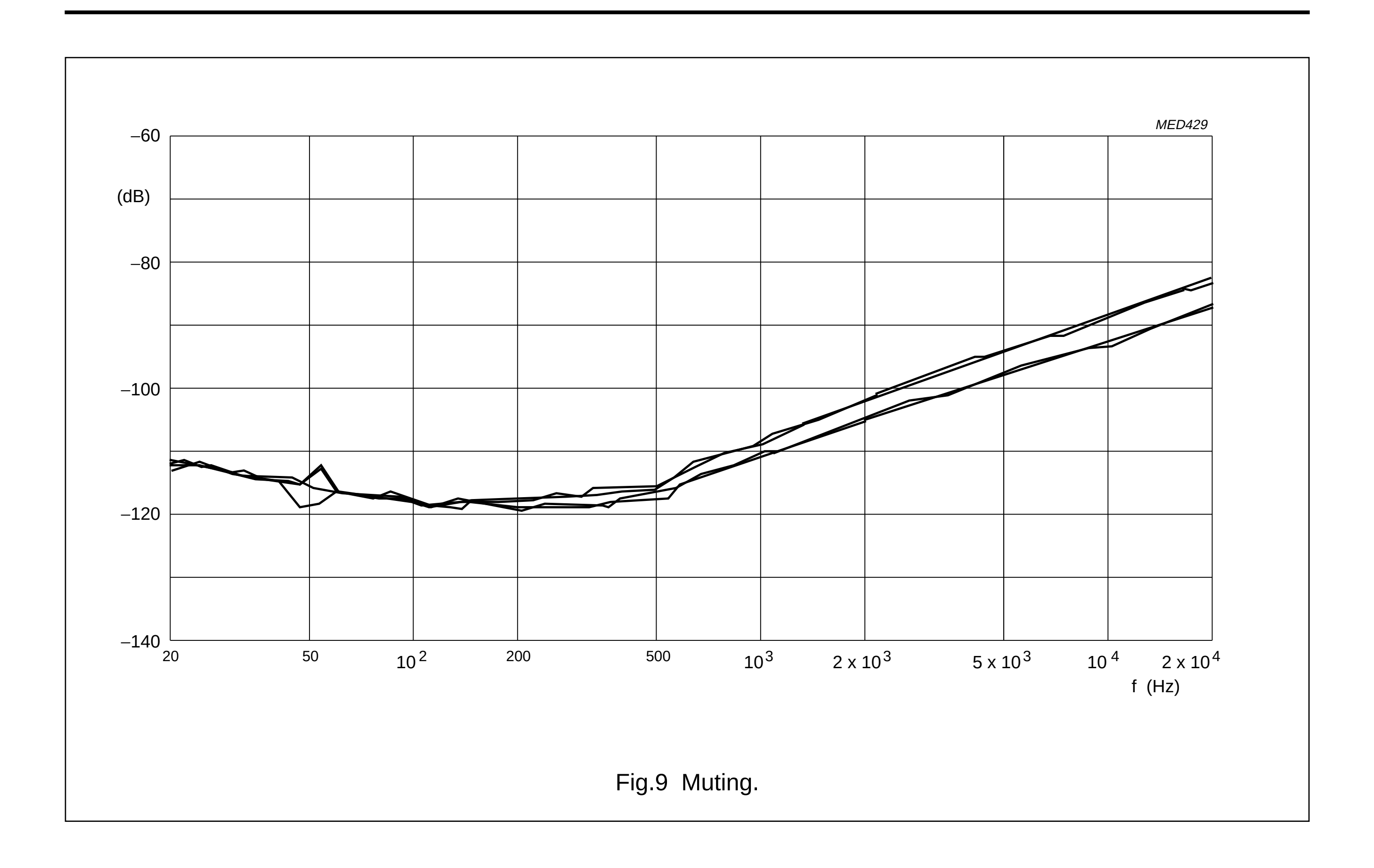
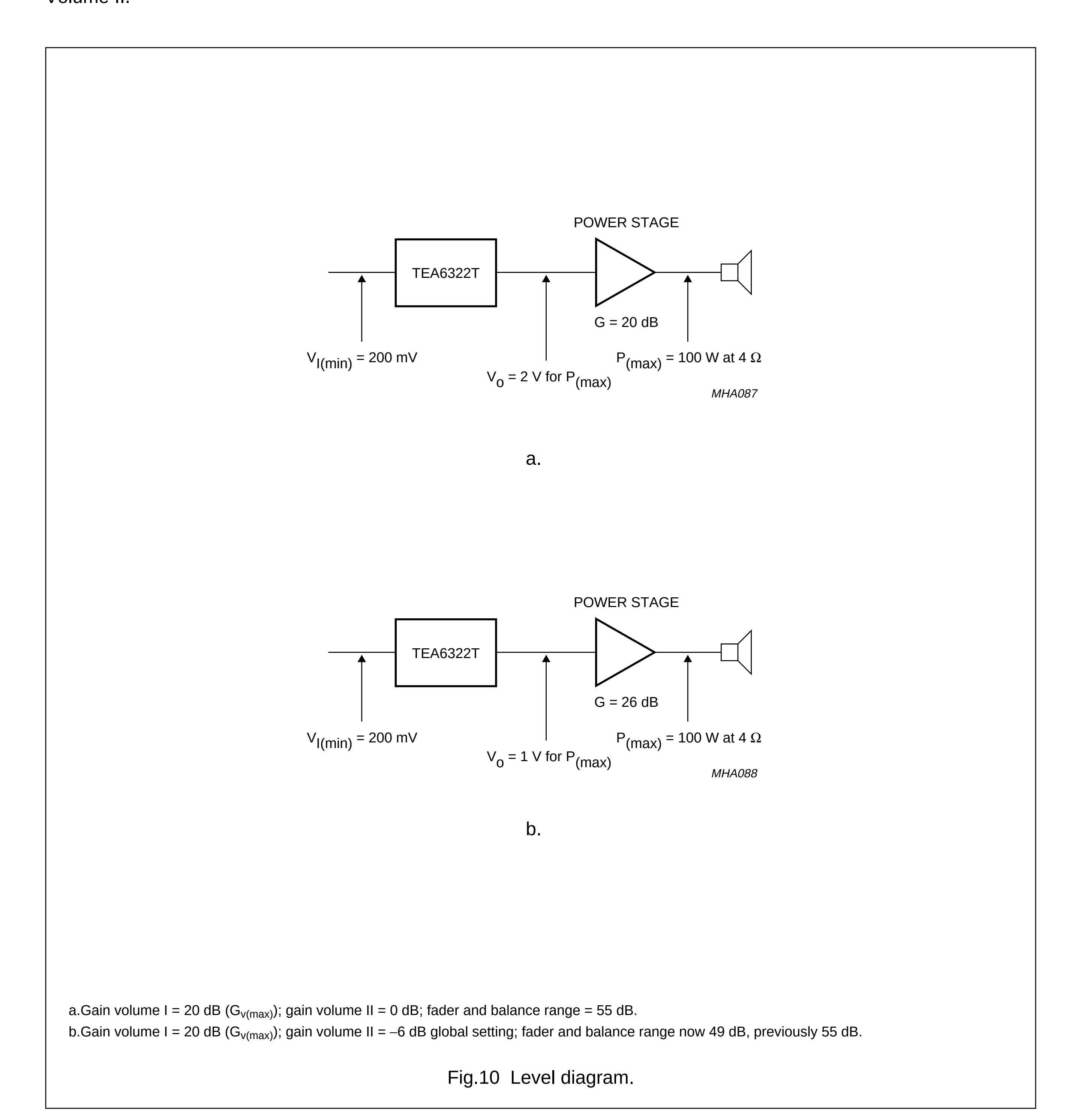

MED429
−60
(dB)
−80
−100
−120
−140
20
50
10 2
200
500
10 3
2 x 10 3
5 x 10 3
10 4
2 x 10 4
f (Hz)

Fig.9 Muting.

If the 20 dB gain is not required for the maximum volume position, it will be an advantage to use the maximum boost gain and then increased attenuation in the last section, Volume II.

Therefore the loudness will be at the correct place and a lower noise and offset voltage will be achieved.

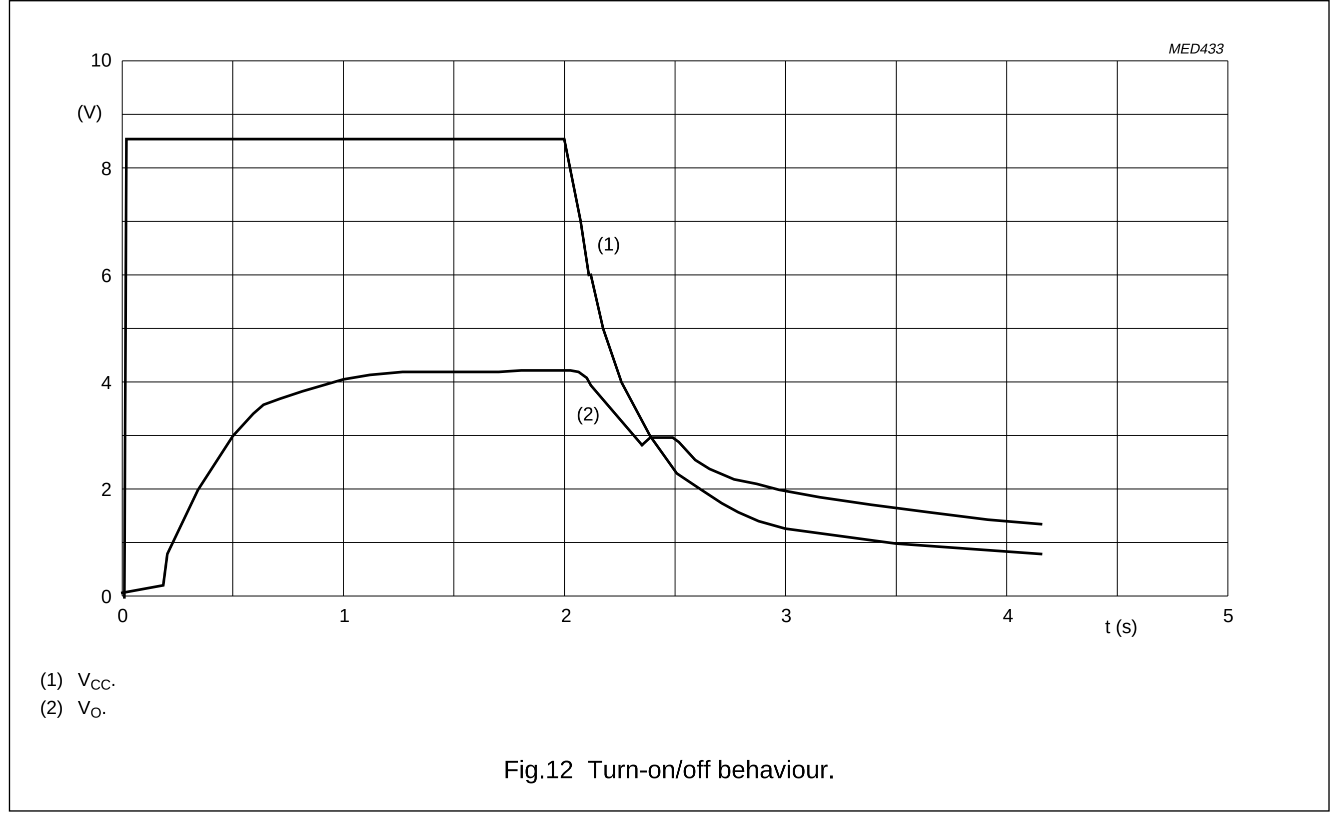


a.Gain volume I = 20 dB ($G_{v(max)}$); gain volume II = 0 dB; fader and balance range = 55 dB.
b.Gain volume I = 20 dB ($G_{v(max)}$); gain volume II = –6 dB global setting; fader and balance range now 49 dB, previously 55 dB.

Fig.10 Level diagram.

V_P
+8.5 V to oscilloscope
V_{CC} 8.5 V
4.7 kΩ
470 µF
inputs
TEA6322T
outputs to oscilloscope
4 × 4.7 µF
9 × 220 nF
9 × 600 Ω
47 µF
100 µF
4 × 10 kΩ
MHA089

Fig.11 Turn-on/off power supply circuit diagram.



(1) V_{CC}.
(2) V_O.

Fig.12 Turn-on/off behaviour.

Fig.13 Test circuit for power supply ripple rejection (RR).

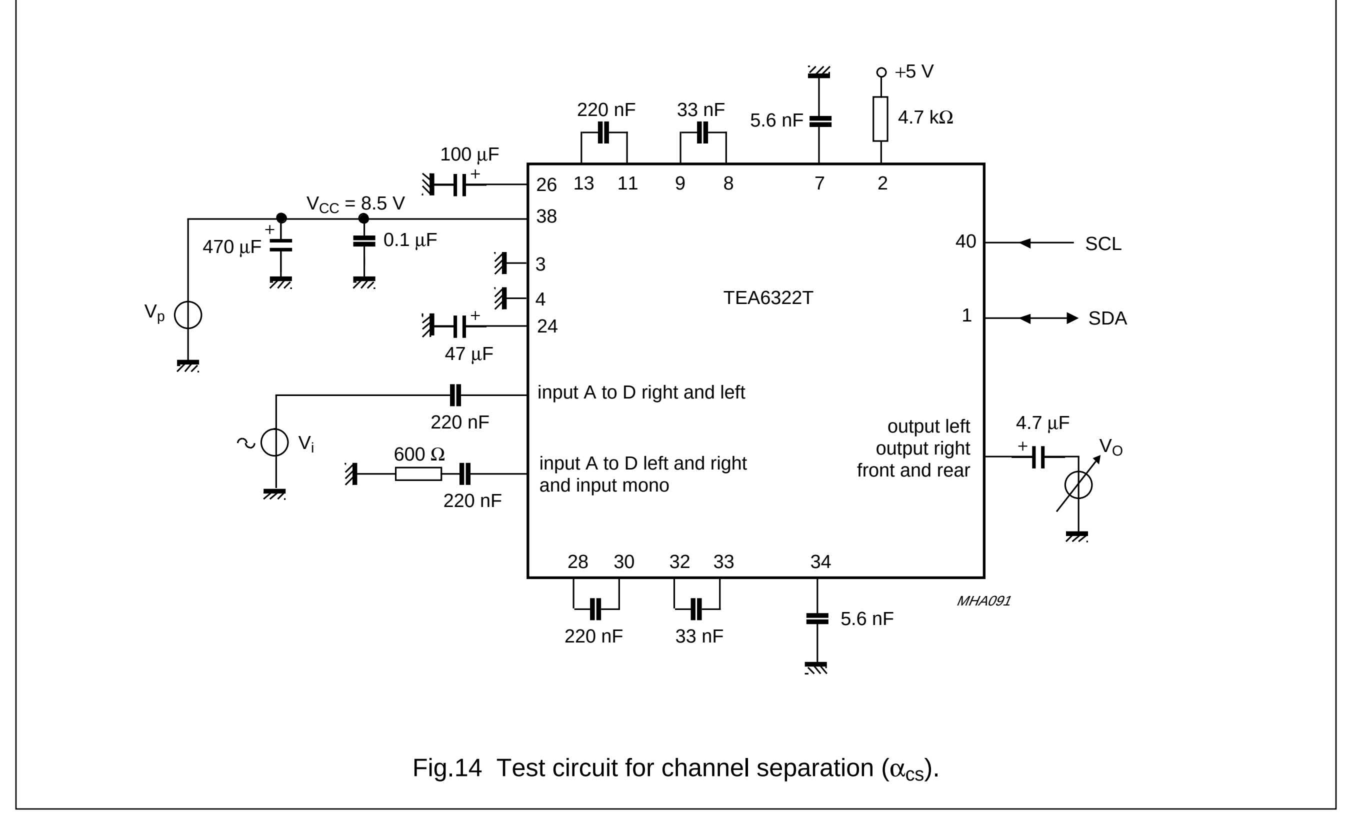


Fig.14 Test circuit for channel separation (α_{cs}).

Loudness filter calculation example

Figure 15 shows the basic loudness circuit with an external low-pass filter application. R1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_2. Both result in a loudness control range of +20 to –12 dB.

Defining f_{ref} as the frequency where the level does not change while switching loudness on/off. The external resistor R3 for $f_{ref} \rightarrow \infty$ can be calculated as:

$$R3 = R1 \frac{10^{\frac{G_v}{20}}}{1 - 10^{\frac{G_v}{20}}}$$

. With G_v = –21 dB and R1 = 33 kΩ,

R3 = 3.2 kΩ is generated.

For the low-pass filter characteristic the value of the external capacitor C1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at f_{ref} as indicated above.

$$\left|\frac{1}{j\omega C_1}\right| = \frac{(R1 + R3) \times 10^{\frac{G_v}{20}} - R3}{1 - 10^{\frac{G_v}{20}}}$$

For example: 3 dB boost at f = 1 kHz
$G_v = G_{v(ref)}$ + 3 dB = –18 dB; f = 1 kHz and C1 = 100 nF.

If a loudness characteristic with additional high frequency boost is desired, an additional high-pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.

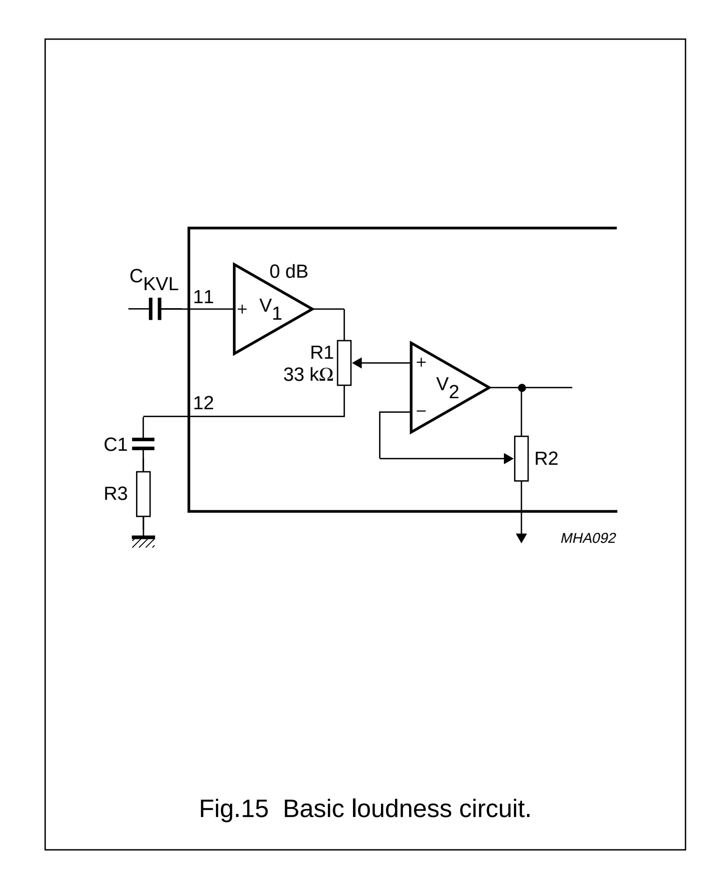


Fig.15 Basic loudness circuit.

INTERNAL PIN CONFIGURATIONS

Values shown in Figs 16 to 28 are typical DC values; V_{CC} = 8.5 V.

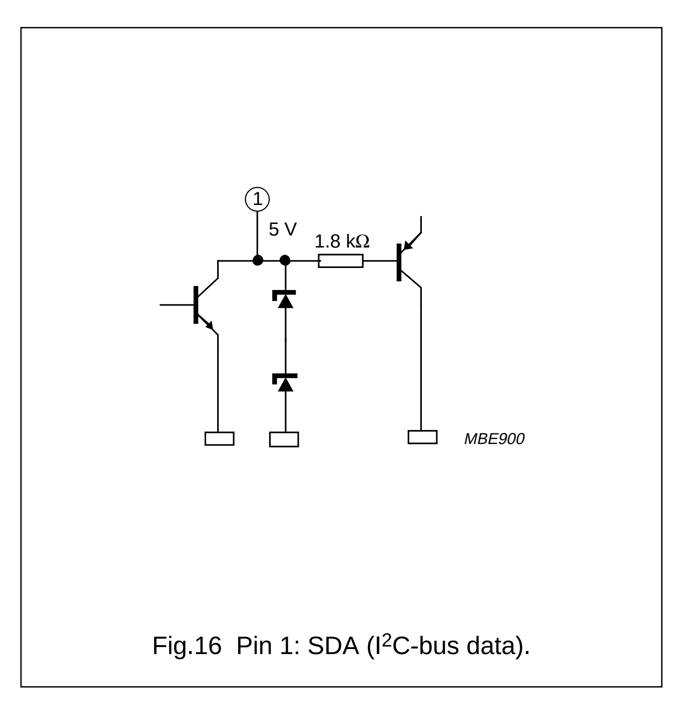


Fig.16 Pin 1: SDA (I²C-bus data).

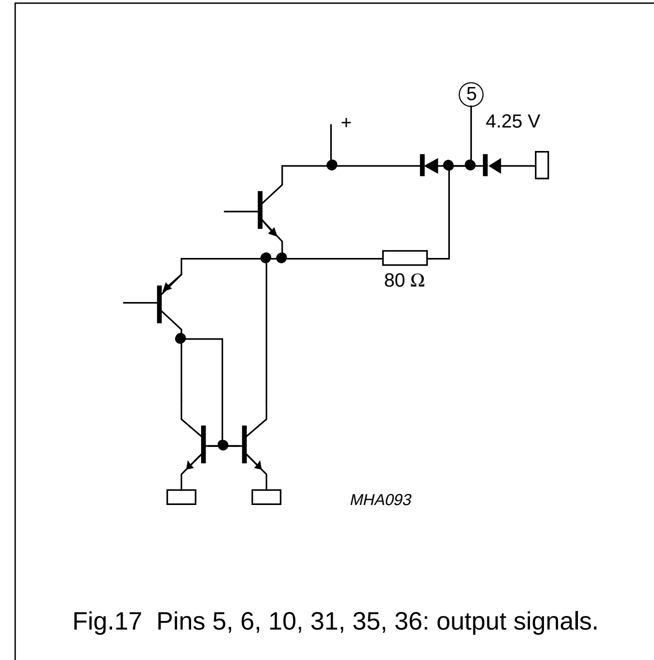


Fig.17 Pins 5, 6, 10, 31, 35, 36: output signals.

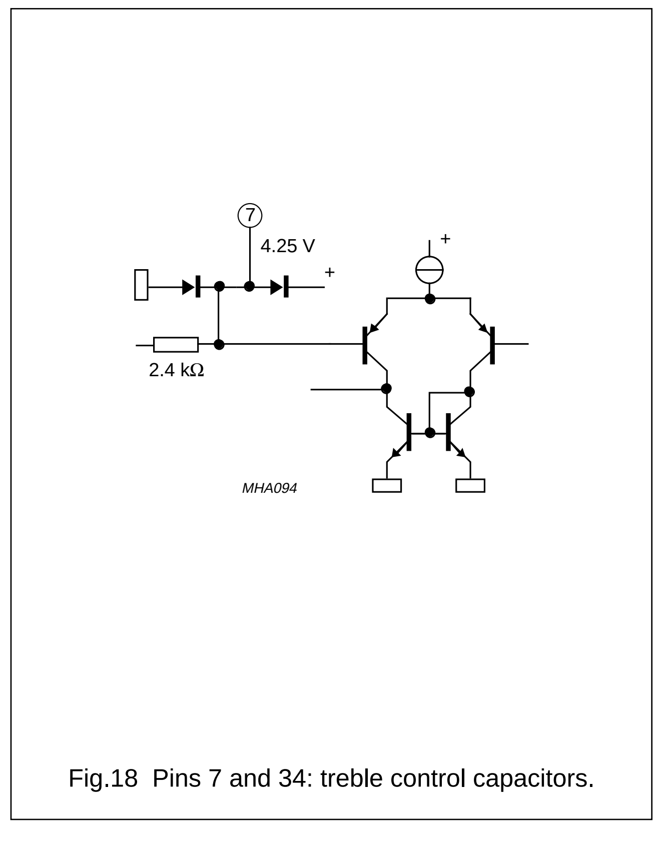


Fig.18 Pins 7 and 34: treble control capacitors.

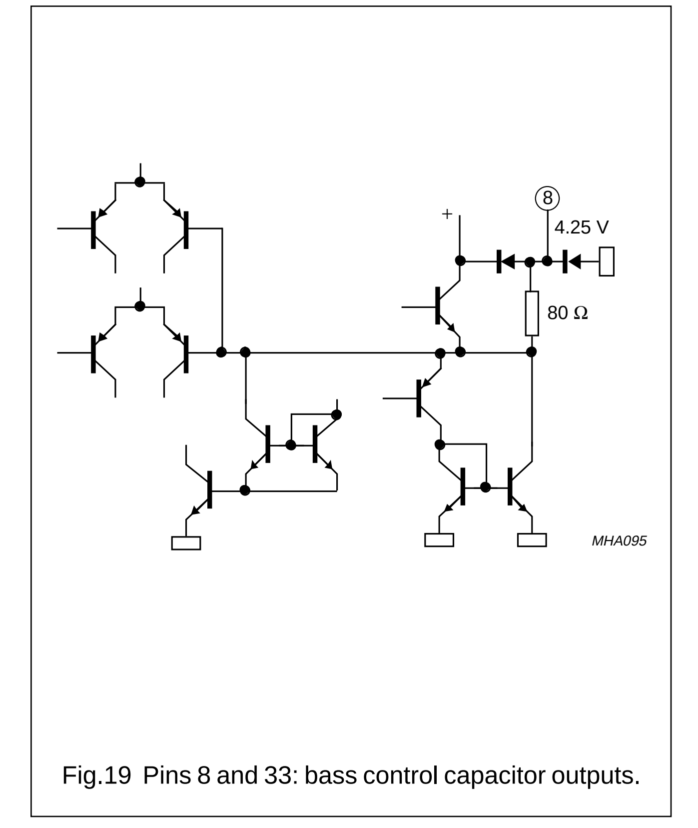


Fig.19 Pins 8 and 33: bass control capacitor outputs.

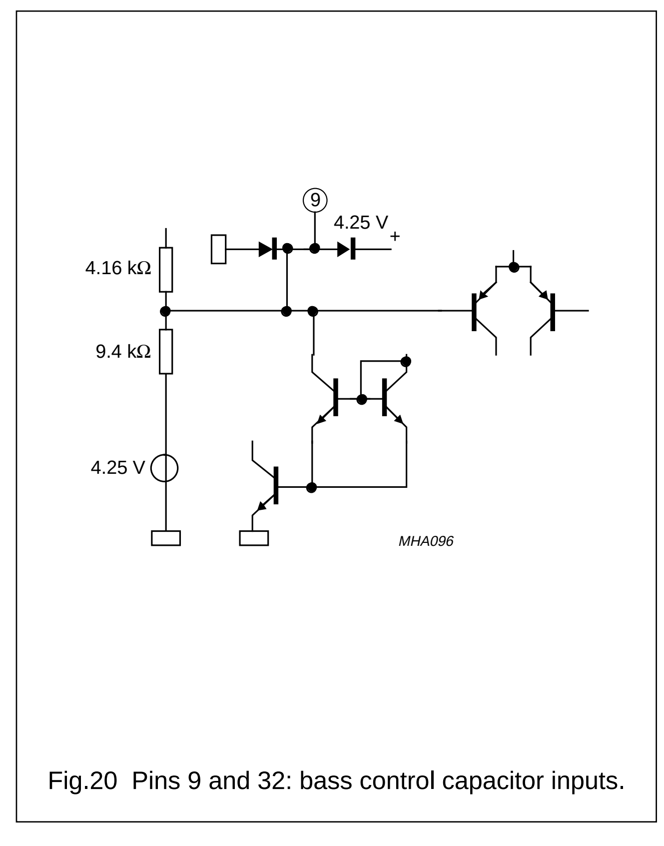


Fig.20 Pins 9 and 32: bass control capacitor inputs.

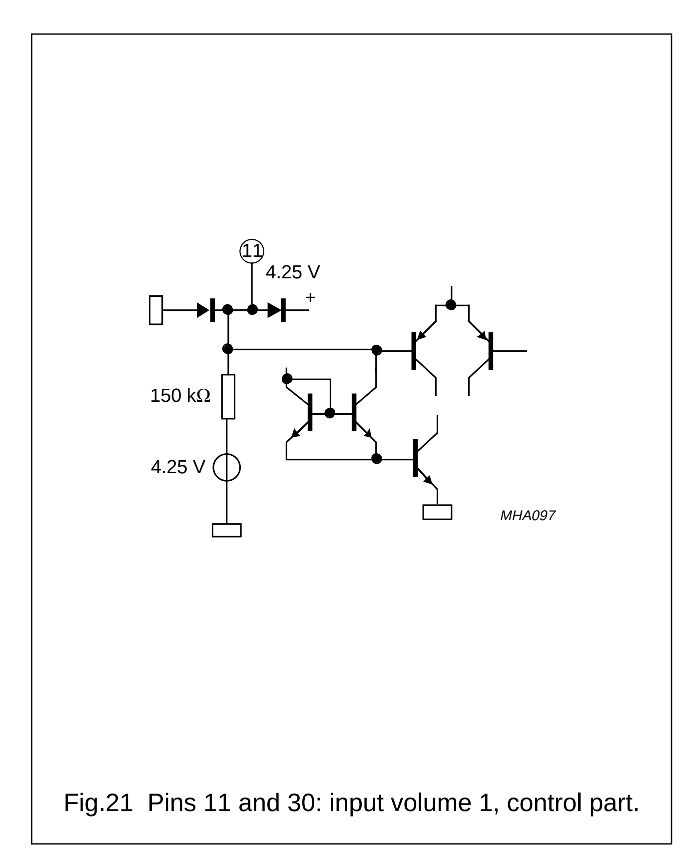


Fig.21 Pins 11 and 30: input volume 1, control part.

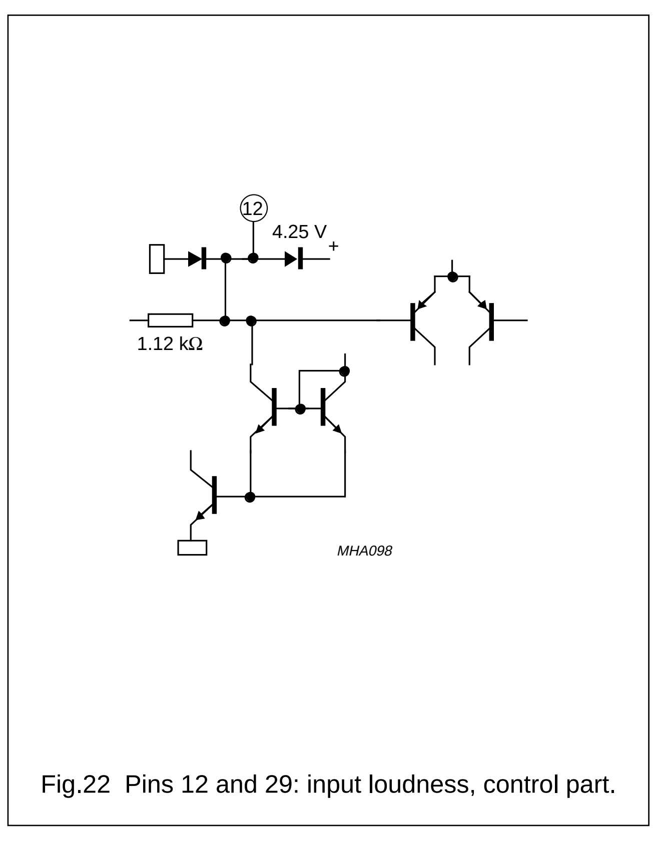


Fig.22 Pins 12 and 29: input loudness, control part.

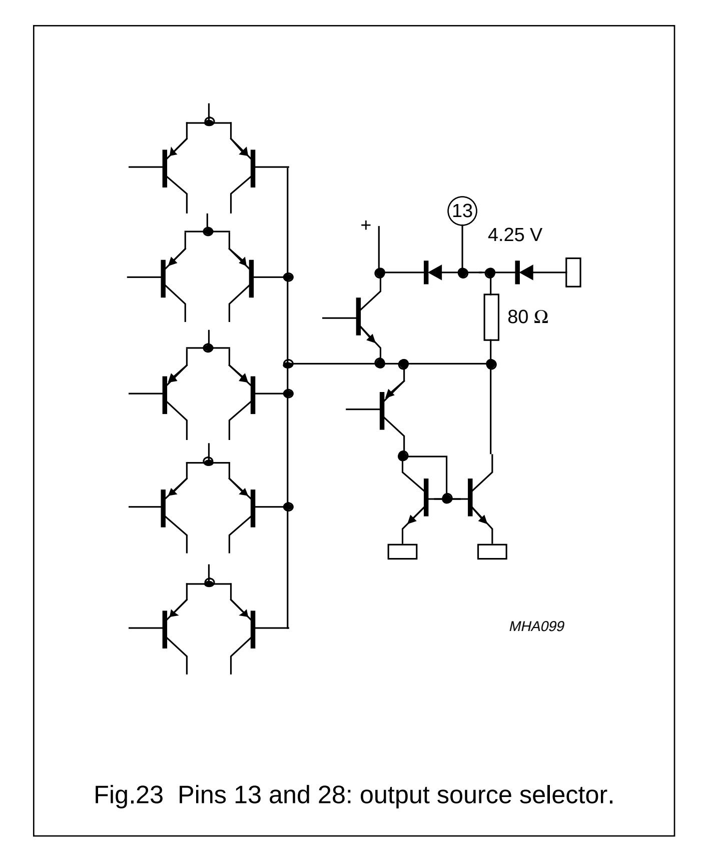


Fig.23 Pins 13 and 28: output source selector.

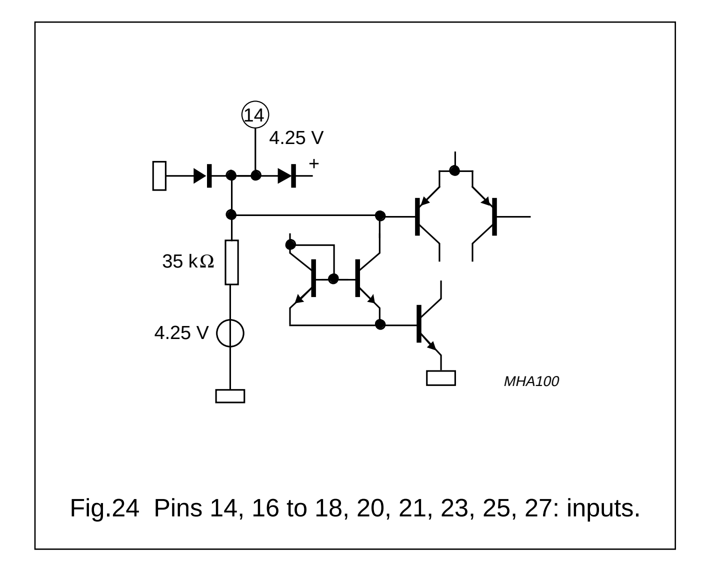


Fig.24 Pins 14, 16 to 18, 20, 21, 23, 25, 27: inputs.

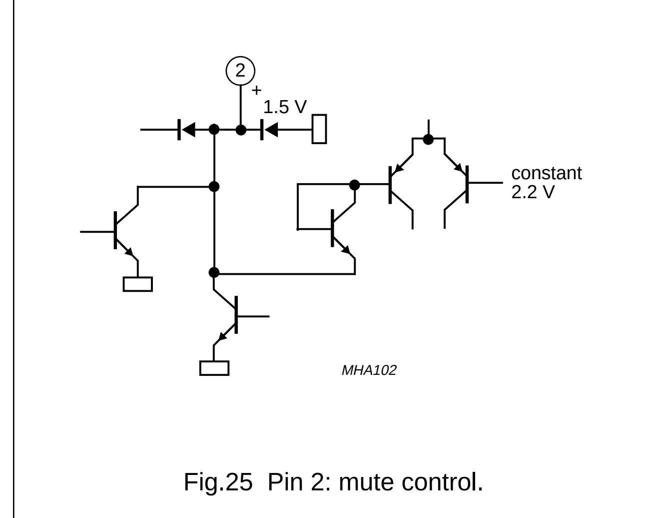


Fig.25 Pin 2: mute control.

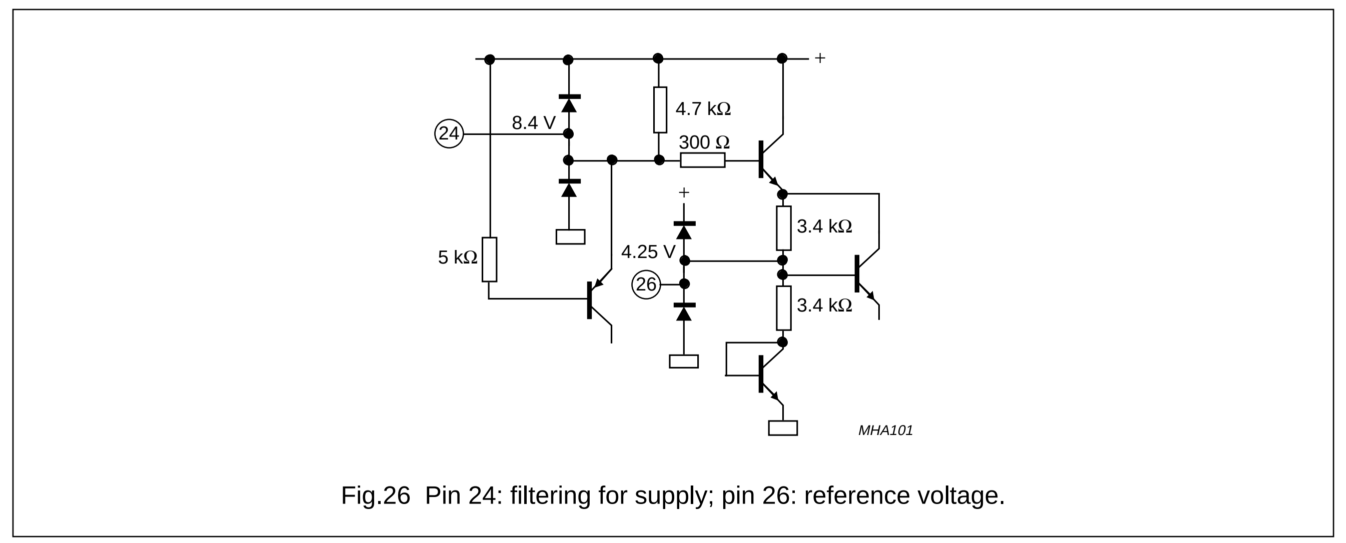


Fig.26 Pin 24: filtering for supply; pin 26: reference voltage.

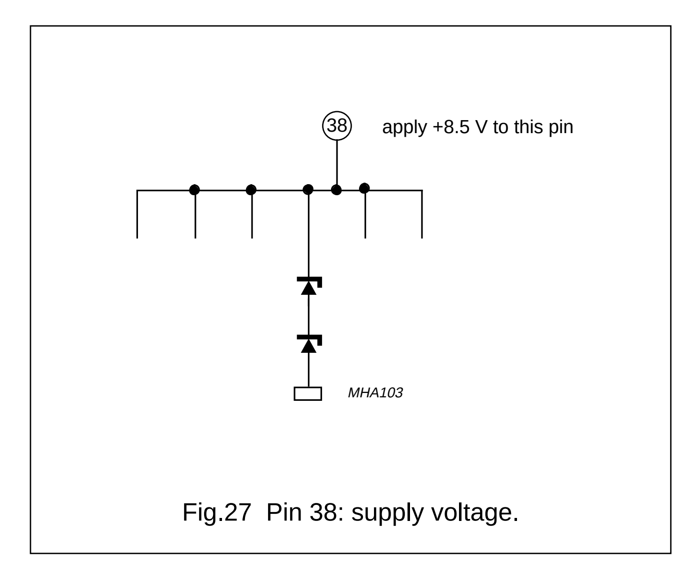


Fig.27 Pin 38: supply voltage.

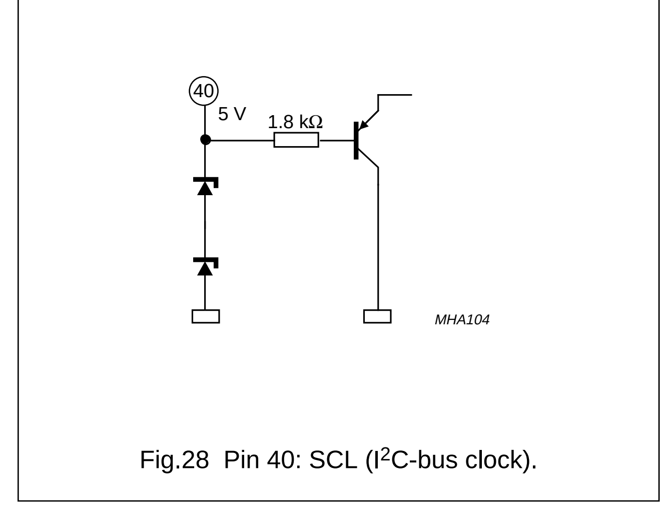
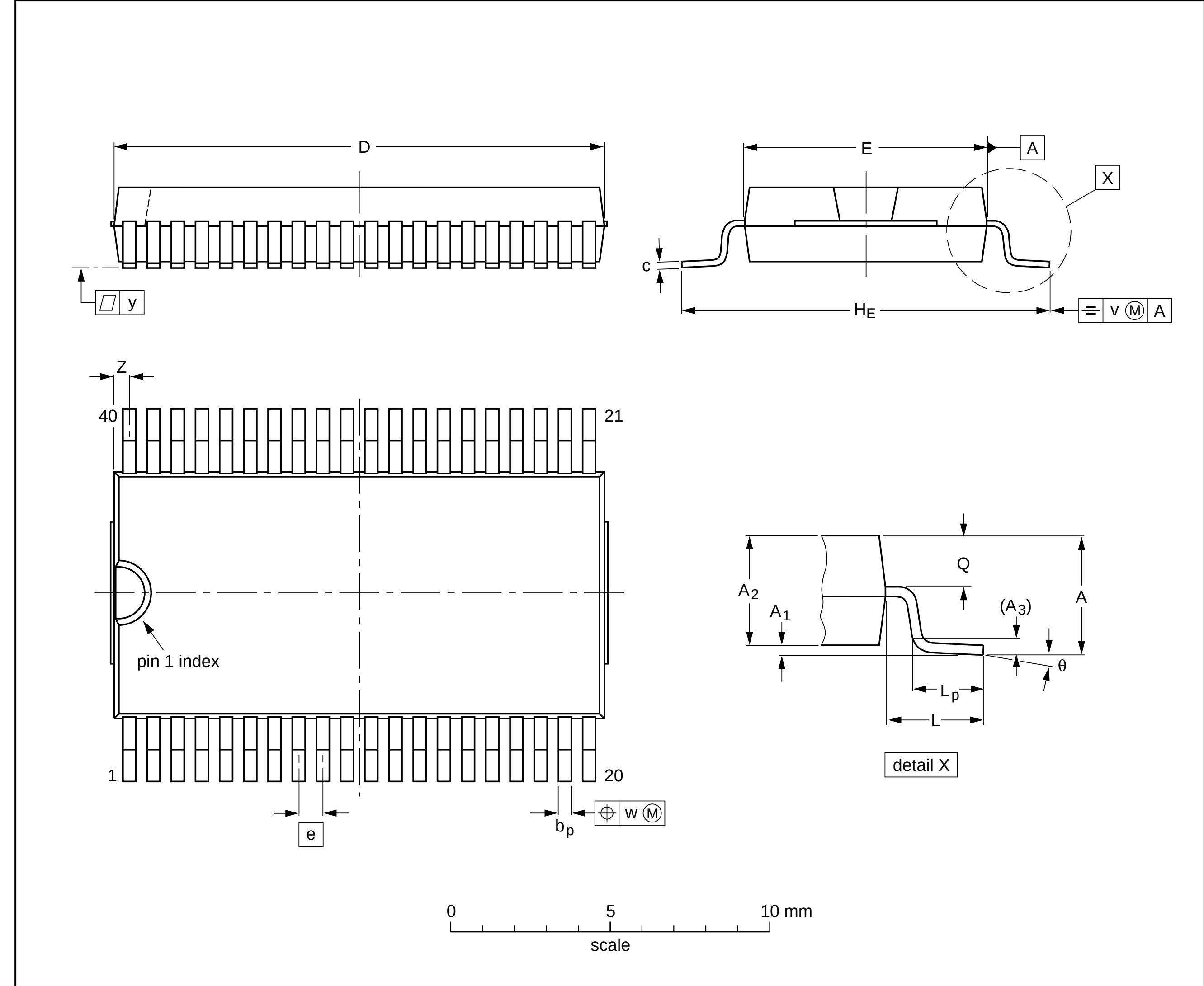


Fig.28 Pin 40: SCL (I^2C-bus clock).

PACKAGE OUTLINE

VSO40: plastic very small outline package; 40 leads **SOT158-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

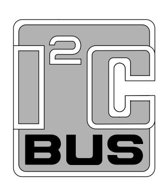
DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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